Motor Encoder Communication Master IP

Under development

Communication master for YASKAWA Electric motor encoders

Overview

Motor Encoder Communication Master IP is an IP that supports YASKAWA Electric encoder communication. This IP transmits data collected from the products that support YASKAWA Electric encoder communication to CPU.

Features

- Collects data from products that support YASKAWA Electric encoder communication by its serial communication link
- Supports Avalon® and APB bus for communication between FPGA and CPU collecting and processing data
- Supports CPU Interrupt

Supported Devices

- Cyclone V

(* Please contact Macnica sales department for information about other devices.)

Deliverables

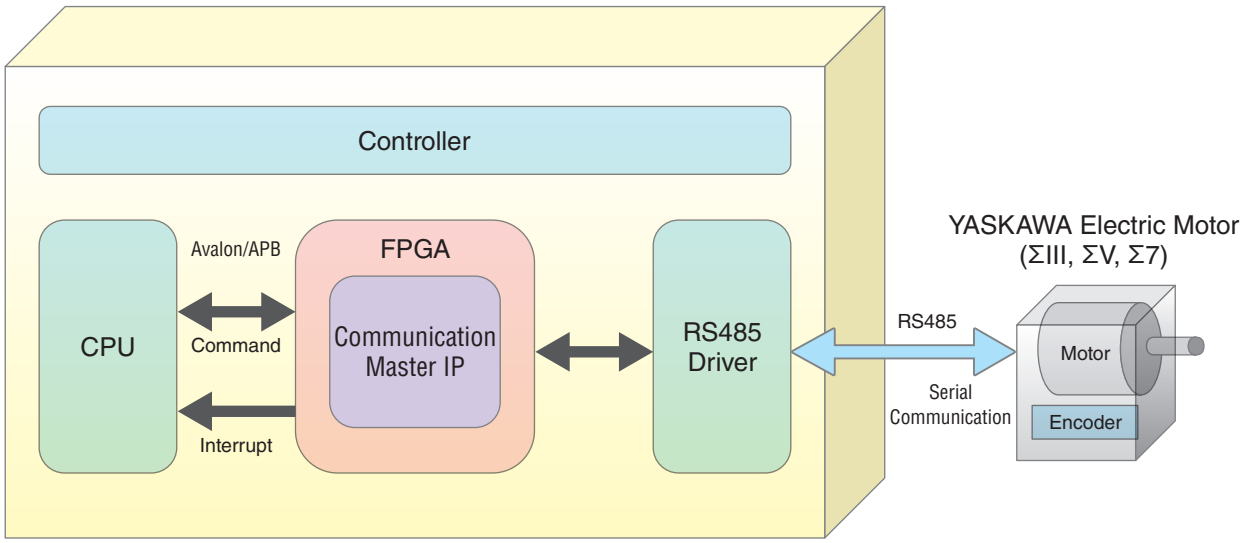
- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- Software library
- Sample software
- User's manual

Device Resource Utilization

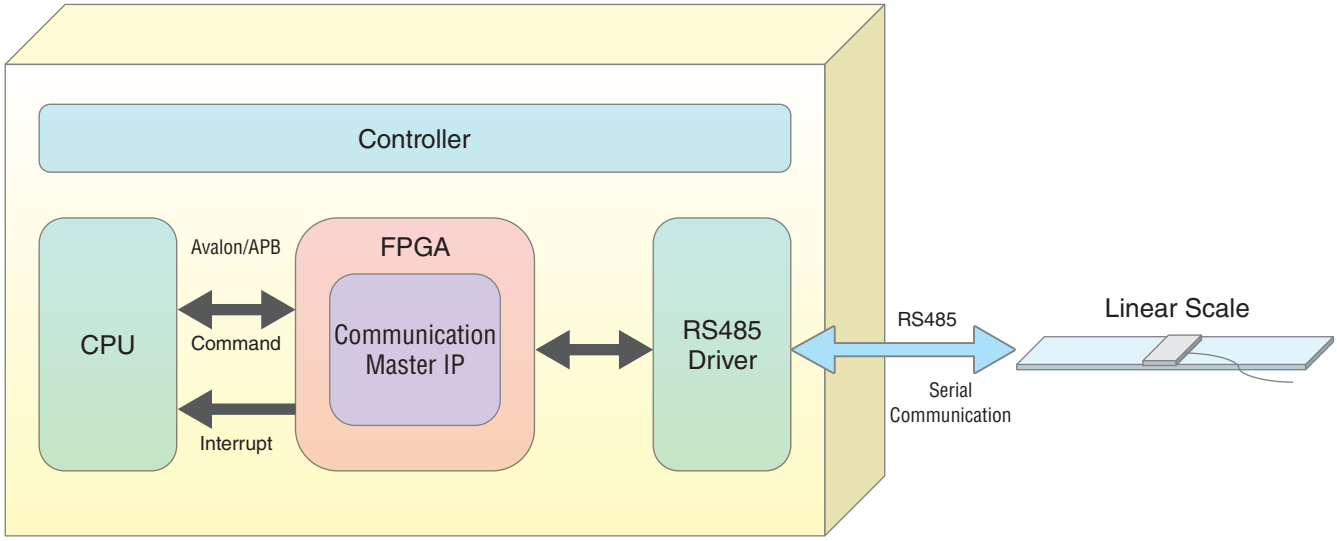
- Cyclone V
  Logic utilization: 3,000 ALMs

Example System Configurations

Example System Configuration 1



Example System Configuration 2



- Transmits data collected from the products that support YASKAWA Electric encoder communication to CPU.
- Interrupts to CPU