

# GigE Vision Device IP Package

High-speed image data transfer complying with GigE Vision standard

## Overview

The GigE Vision Device IP Package is an IP package to transfer image data complying with GigE Vision standard. The IP transmits image data from the image sensor to Gigabit Ethernet in real time. Users can build highly reliable products making use of its high-speed transfer capability and high-precision time synchronization. Perfect for high-resolution, high-reliable machine vision cameras, medical imaging systems, and other applications that demand maximized Gigabit Ethernet performance.

## Features

- Highly reliable image transmission using GigE Vision protocol
- 995 Mbps maximum effective transfer rate
- Comprehensive reference environment
- GigE Vision Compliant, Certified by AIA with Logo
- Interoperability qualified with various GenICam application vendors
- Support IEEE1588 PTP as Master and Slave

## Specifications

- Compliant with GigE Vision Standard Version 1.2/Version 2.0
- Supports IEEE1588-2008 PTP
- Compliant with EMVA GenICam Standard Version 2.0
- Supports Packet Re-transmission
- Other functions
  - Chunk data transfer, GigE Vision action commands, Time stamp, Packet delay
  - Image data (RGB, YUV, etc.) and RAW data transfer

## Supported Devices

- Cyclone III/IV/V
- (\* Please contact Macnica sales department about other devices.)

## Deliverables

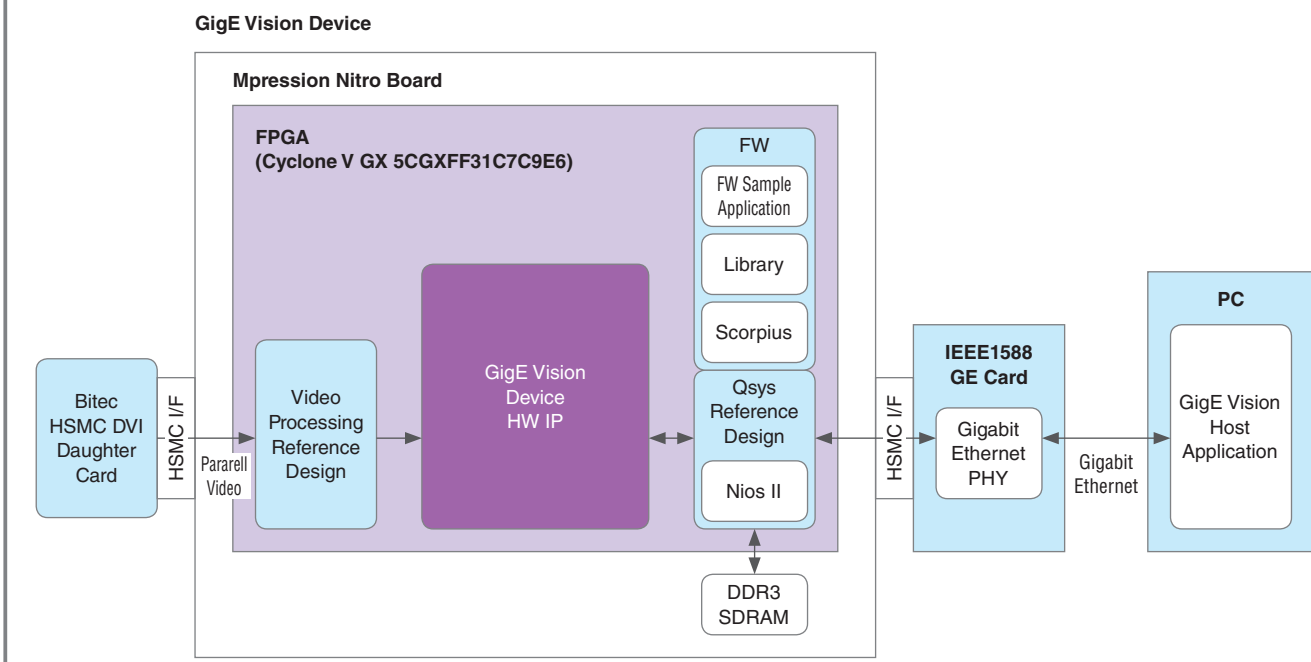
- Encrypted RTL (Verilog HDL)
  - GigE Vision Device FW Library for Nios II processors
  - Reference environment (sample hardware design, firmware application)
  - User's manual
- (\* Please contact Macnica sales department about other deliverables.)

## Device Resource Utilization

- |   |  |
|---|--|
| <ul style="list-style-type: none"><li>• Cyclone III<ul style="list-style-type: none"><li>- Total logic elements : 47,608</li><li>- Total registers : 28,673</li><li>- Total memory bits : 782,892</li></ul></li></ul> | <ul style="list-style-type: none"><li>• Cyclone V<ul style="list-style-type: none"><li>- Logic utilization (in ALMs) : 21,235</li><li>- Total registers : 34,592</li><li>- Total block memory bits : 1,244,592</li></ul></li></ul> |
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\* The values in the above table are based on an implementation example. There may be some variation depending on the user's system configuration.

## System Block Diagram



## Evaluation Environment

Category	Product Name	Vendor
(1) Base Board	Nitro – Cyclone V GX I/O Expansion Base Board	Mpression
(2) Daughter Card	IEEE1588 GE Card	Mpression
(3) Daughter Card	HSMC DVI Digital Video Daughter Card	Bitec
(4) Host Application	GenICam Software	Mpression

