SLVS-EC Rx IP

Next Generation Sony CMOS image sensor interface

Overview

SLVS-EC Rx IP provides SLVS-EC interface for Altera FPGA to receive image sensor data. SLVS-EC is Sony's upcoming high-speed interface for next-generation high-resolution CMOS image sensors.
This standard is tolerant of lane-to-lane skew because of embedded clock technology, so that it makes a board level design very easy in terms of high-speed and long distance transmission.

Features

- Compliant with SLVS-EC Specification Version 1.2
- Supports various functions defined by the SLVS-EC Link layer (Altera PCS/PMA is used as Physical layer)
- Supports Byte-to-Pixel conversion for various lane-configurations
- Supports Header analysis and Payload error detection

Specifications

Function	SLVS-EC Rx IP Support
Number of Lanes	1,2,4,6,8
Baud Grade	1,2
Bit per Pixel	8,10,12,14
CRC	Limited *
ECC	Not Supported
Embedded Data	Supported
Dynamic Mode Change	Supported
Multiple Stream	If needed

* The operating frequency may not be achievable depending on the speed grade, number of lanes, and other factors of the FPGA used. Please contact Macnica sales department for information about limitations.

Supported Devices

- ALTERA Cyclone® V GX
- ALTERA Arria®10 GX

* Please contact Macnica sales department for information about other devices.

Deliverables

- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- User's manual, Reference manual

Device Resource Utilization

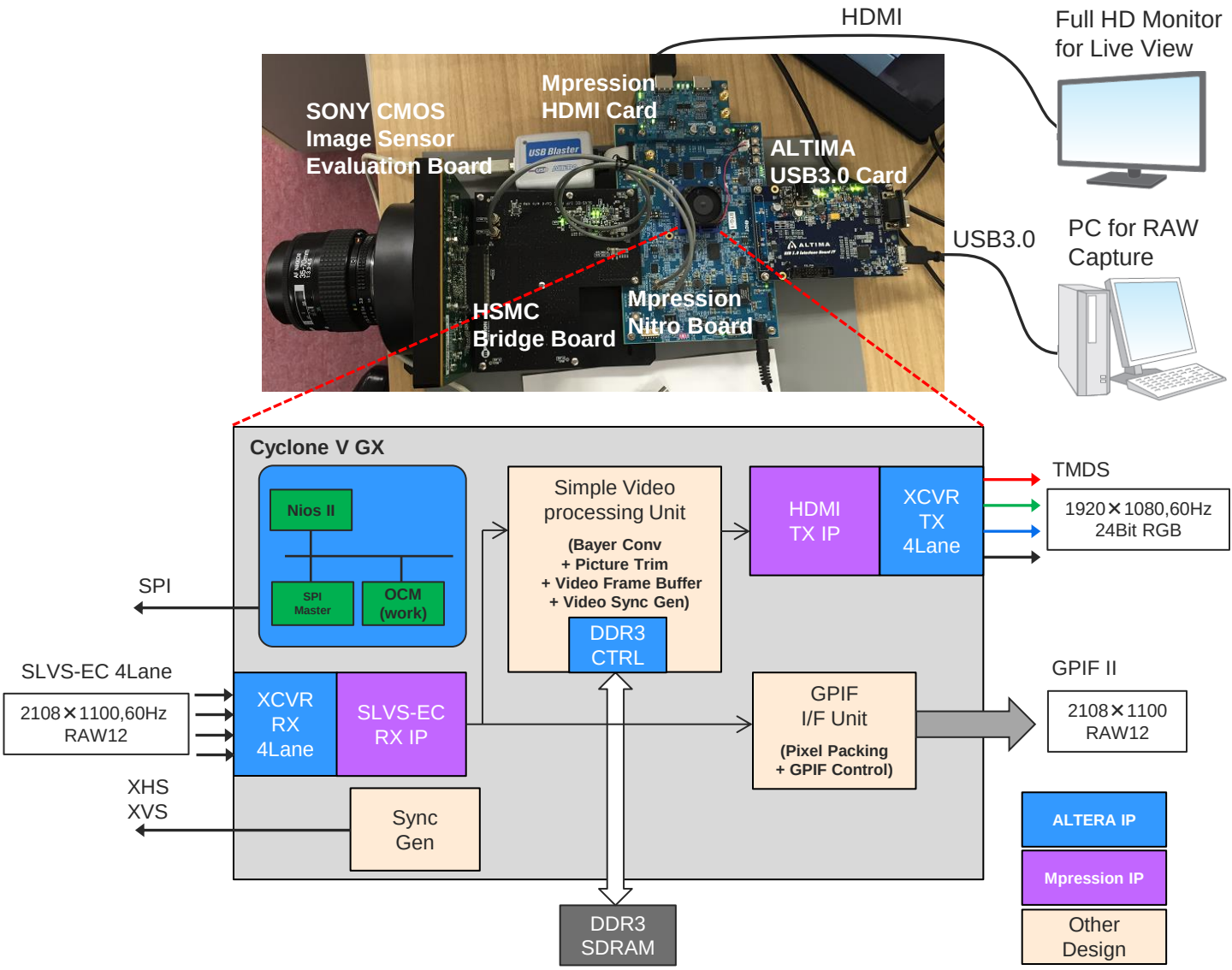
Resource Utilization in case of 8 LANE Full Configuration

Items	Cyclone V	Arria 10
ALMs	4485	3910
Total registers	4316	3751
Total block memory bits	4096	2560

* The above values are estimated resource utilization of the IP and Transceivers. They may vary depending on your system configuration.

Demo Environment

Data output from Sony CMOS image sensor via SLVS-EC is received by the FPGA. The FPGA outputs RAW still image to USB3.0 and live video image to HDMI respectively.
In addition to SLVS-EC Rx IP, another Mpression family IP, “HDMI 2.0 Tx IP” is also used in this demonstration.



* This demo design is not included in the deliverables.

Other

- Please contact Macnica Sales Department for electrical characterization for Intel FPGA devices regarding SLVS-EC specifications.

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