V-by-One HS Tx/Rx IP

High-speed serial interface compliant with V-by-One HS standard

Overview

V-by-One HS Tx/Rx IP is an IP to achieve V-by-One HS high-speed video interface technology. V-by-One HS is a standard for next-generation high-speed interface technology developed by THine Electronics for image and video equipment requiring higher frame rates and higher resolutions. Implementing the V-by-One HS Tx/Rx IP in Intel FPGA reduces the number of signals compared with conventional LVDS interfaces, which greatly reduces product cost.

Features

- Achieves 4-Gbps maximum transmission rate per lane (however, depends on the FPGA used)
- Supports custom video formats as well as VESA, SMPTE, and other standardized formats
- Supports flexible multi-lane designs in accordance with user’s total transmission rate requirement
- Self-check function (FieldBET) to test connectivity between transmitter and receiver IPs

Specifications

<table>
<thead>
<tr>
<th></th>
<th>Transmitter IP</th>
<th>Receiver IP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lane</td>
<td>1 to 32</td>
<td>FieldBET Pattern Generator</td>
</tr>
<tr>
<td>Pixel Data</td>
<td>24, 32, 40 bit</td>
<td>FieldBET Pattern Checker</td>
</tr>
</tbody>
</table>

Supported Devices

- Cyclone® IV GX
- Cyclone V GX/GT
- Cyclone 10 GX
- Arria® II GX
- Arria V GX
- Arria 10 GX
- Stratix® IV GX
- Stratix V GX

(* Please contact Macnica sales department about other devices.)

Deliverables

- Encrypted RTL (Verilog HDL)
- Reference design
- Simulation environment (For ModelSim)
- User’s manual
- Reference design user’s guide

Device Resource Utilization

<table>
<thead>
<tr>
<th>IP</th>
<th>Lane</th>
<th>Cyclone IV GX</th>
<th>Arria IV GX</th>
<th>Stratix IV GX</th>
<th>Stratix V GX</th>
<th>Arria 10 GX</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>LE</td>
<td>Register</td>
<td>Block Memory</td>
<td>ALUT</td>
<td>Register</td>
</tr>
<tr>
<td><strong>TX</strong></td>
<td>2</td>
<td>3,946</td>
<td>2,782</td>
<td>0</td>
<td>1,933</td>
<td>2,782</td>
</tr>
<tr>
<td><strong>RX</strong></td>
<td>2</td>
<td>6,477</td>
<td>4,949</td>
<td>0</td>
<td>2,574</td>
<td>4,949</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Cyclone V GX</td>
<td>Arria V GX</td>
<td>Stratix V GX</td>
<td>Arria 10 GX</td>
<td></td>
</tr>
<tr>
<td><strong>TX</strong></td>
<td>2</td>
<td>1,598</td>
<td>2,977</td>
<td>0</td>
<td>1,603</td>
<td>2,964</td>
</tr>
<tr>
<td><strong>RX</strong></td>
<td>2</td>
<td>2,273</td>
<td>5,416</td>
<td>0</td>
<td>2,274</td>
<td>5,377</td>
</tr>
</tbody>
</table>

* The values in the above table are based on an implementation example. There may be some variation depending on the user’s system configuration.
### Configuration Diagram

- **VX1 RX**
- **VX1 TX Core** (lane N)
- **PLL**
- **User Logic**
- **Lane Mapped Video I/F**
- **D/K Code I/F**
- **Transmitter PHY**
- **CML (lane 1)**
- **CML (lane N)**
- **HTPDN**
- **LOCKN**
- **Receiver PHY**
- **VX1 RX Core** (lane 1)
- **Lane De-skew**
- **VX1 TX Core** (lane 1)
- **(FPGA)**
- **PLL**

### Evaluation Environment

- **LCD Display**
- **DVI cable**
- **Media Player**
- **(1080p 60Hz)**
- **VX1-DVI FMC Card**

### Evaluation Board

<table>
<thead>
<tr>
<th>Category</th>
<th>Product Name</th>
<th>Vendor</th>
</tr>
</thead>
<tbody>
<tr>
<td>Main Board</td>
<td>Arria 10 GX FPGA Development Kit</td>
<td>Intel</td>
</tr>
<tr>
<td>Daughter Card</td>
<td>V-by-One HS DVI FMC Card</td>
<td>Mpression</td>
</tr>
</tbody>
</table>

**VX1: V-by-One HS**